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09/639,753	08/15/2000	Takehiro Ohkawa	NIT-217	4173

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EXAMINER	
YANG, CLARA I	

ART UNIT	PAPER NUMBER
2635	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/639,753	OHKAWA ET AL.	
	Examiner	Art Unit	
	Clara Yang	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 22 January 2004 have been fully considered but they are not persuasive. The applicant argues on page 2 that "the voltage level of the data carrier 200 is fixed to VDD (High)" when switch 15 of Hanaoka's data carrier 200 is off, causing T1 to open. The Examiner respectfully disagrees with the applicant for the following reasons and maintains the previous rejections.

Hanaoka's teaches that transistor T1 is a p-channel metal-oxide-semiconductor (MOS) transistor (see Col. 12, lines 1 - 2), and one of ordinary skill in the art recognizes that T1's switching characteristic is controlled by its gate, not by V_{DD}. As disclosed by Hanaoka, data carrier main circuit 100, which is connected to transistor T1's gate, turns transistor T1 on and off in order to superimpose data onto the current flowing to coil 1 (see Fig. 8 and Col. 12, lines 2 - 5). Because transistor T1 is a p-channel MOS transistor, when data carrier main circuit 100's output is low (i.e., logic 0), transistor T1 is closed (or "on"), causing the circuit impedance to be low. Likewise, when data carrier main circuit 100's output is high (i.e., logic 1), transistor T1 is open (or "off"), causing the circuit impedance to be high. Data carrier main circuit 100, in turn, is turned on or off by transistor T4, which is an n-channel MOS transistor. Per Hanaoka, when voltage V_{S1} decreases below the lowest operation voltage V_{off}, voltage detector circuit 13's second amplifier (or transistor T3) changes its output to logic 0, and the switch control singles S_S changes to logic 0 to turn off transistor T4, thus stopping the supply of power to power source line V_{S2} and deactivating data carrier main circuit 100. (See Col. 13, lines 5 - 16.) It is understood that data carrier main circuit 100's output becomes low (or logic 0) when it is turned

off (or in a reset state), causing transistor T1 to close and to maintain data carrier 200's circuit in a low impedance state.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4 - 8, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,521,590 (Hanaoka et al.).

Referring to Claims 1 and 4, Hanaoka's data carrier 200 or radio frequency identification (RFID) device, as shown in Figs. 4 and 5, comprises: (a) coil 1, i.e. "antenna", for receiving power to drive modulator circuit 2 and data carrier main circuit 100, i.e. "semiconductor circuit device", and for transmitting and receiving signals (see Col. 9, lines 50 - 54 and Col. 11, lines 7 - 19); and (b) voltage detector circuit 13 and switch 15, i.e. "first means", for releasing inner elements of data carrier main circuit 100 from an inactive state and putting the inner elements in an active state upon detection that the DC voltage supplied by rectifier circuit 4 is higher than a predetermined voltage (see Col. 9, lines 55 - 65 and Col. 10, lines 9 - 27 and 58 - 67). When voltage detector circuit 13 determines that DC voltage supplied by rectifier circuit 4 is a predetermined voltage, circuit 13 closes switch 15, thus supplying the voltage to activate power-on reset circuit 14 (see Col. 10, lines 18 - 23 and 58 - 64). Power-on reset circuit 14 initializes control circuit 10 (see Col. 10, lines 24 - 25 and 64 - 67 and Col. 11, lines 1 - 3). When data carrier 200 receives a command to send data read from memory circuit 9, Hanaoka teaches that

modulator circuit 2 changes the impedance between the induced voltage line V_{ac} and the reference potential line V_{dd} according to the data ($DATA_{out}$) read from memory circuit 9, thus resulting in changing an AC magnetic field emitted from coil 1 (see Col. 11, lines 14 - 19). As shown in Fig. 8, modulator circuit 2 includes transistor T1, which is a p-channel metal-oxide-semiconductor (MOS) transistor (see Col. 12, lines 1 - 2). Per Hanaoka, data carrier main circuit 100, which is connected to transistor T1's gate, turns transistor T1 on and off in order to superimpose data onto the current flowing to coil 1 (see Fig. 8 and Col. 12, lines 2 - 5). Because transistor T1 is a p-channel MOS transistor, when data carrier main circuit 100's output is low (i.e., logic 0), transistor T1 is closed (or "on"), causing the circuit impedance to be low. Likewise, when data carrier main circuit 100's output is high (i.e., logic 1), transistor T1 is open (or "off"), causing the circuit impedance to be high. In addition, Hanaoka imparts that when the DC voltage from rectifier circuit 4 is below a predetermined value, voltage detector circuit 13 provides a switch control signal to turn off switch 15 so that no power is supplied to data carrier main circuit 100, thereby putting data carrier main circuit 100 in a reset state (see Col. 10, lines 58 - 62). It is understood that data carrier main circuit 100's output becomes low (or logic 0) when it is turned off (or in a reset state), causing transistor T1 to close and to maintain data carrier 200's circuit in a low impedance state.

Regarding Claim 2, as an example, Hanaoka discloses that the voltage levels to turn on and off power-on reset circuit 14 are set to 1.5 V and 1.2 V in voltage detector circuit 13 respectively (see Col. 7, lines 7 - 16 and Col. 14, lines 24 - 27). Because Hanaoka, voltage detector circuit 13 checks the voltage to see whether or not the voltage is sufficiently large to stably operate data carrier main circuit 100, it is understood that data carrier main circuit 100's guarantee working voltage is around 1.2 V.

Referring to Claims 5 - 8, because Hanaoka imparts in Col. 1, lines 5 - 9, that data carrier 200 includes non-contact IC cards, it is understood that components 2 - 10 and 13 - 15 of data carrier 200 of RFID device, as shown in Figs. 4 and 5, form an integrated circuit element. Hanaoka's integrated circuit element comprises: modulator circuit 2 or communication means, MONOS memory circuit 9 or memory means, control circuit 10 or logic processing means, and power-on reset circuit 14 for releasing control circuit 10 from an inactive state (see Col. 9, lines 62 - 65; Col. 10, lines 24 - 25 and 67; and Col. 11, lines 1 - 3). Hanaoka's data carrier 200 further comprises coil 1 for receiving power and signals from an external apparatus and for supplying power and signals to memory circuit 9 and control circuit 10 (see Col. 9, lines 50 - 54 and Col. 11, lines 7 - 19). When a voltage applied to power-on reset circuit 14 is lower than a threshold value, voltage detector circuit 13 causes switch 15 to cease supplying power to data carrier main circuit 100, causing data carrier 200 to become inactive (see Col. 10, lines 58 - 62). When data carrier 200 is inactive, its impedance state is low state for the reasons explained above in claims 1 and 4. When a reset state is released, signal transmission is performed by modulator circuit 2 changing the impedance between the induced voltage line V_{ac} and the reference potential line V_{dd} according to the data ($DATA_{out}$) read from memory circuit 9, thus resulting in changing an AC magnetic field emitted from coil 1 (see Col. 11, lines 14 - 19).

Regarding Claim 11, Hanaoka states that data carrier 200 includes non-contact integrated circuit (IC) cards (see Col. 1, lines 5 - 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,521,590 (Hanaoka et al.) as applied to claim 1 above, and further in view of U.S. Patent No. 6,246,624 (Hirano et al.).

Hanaoka omits teaching a reset voltage for activating data carrier 200 that is equal to the reset voltage for deactivating data carrier 200.

In an analogous art, Hirano teaches an RFID tag having a voltage detection circuit and a power-on/off reset circuit (see Col. 13, lines 10 - 15). In order to properly terminate a sequence in operation of a memory circuit, Hirano discloses a power-on/off reset circuit as shown in Fig. 13. Hirano's power-on/off reset circuit has voltage detection circuit 42 and 43. Voltage detection circuit 43 controls internal control signal (ICE) control circuit 45, and voltage detection circuit 42 controls word line (WL), cell plate line signal (CP), and sense amplifier enable signal (SAE) control circuit 44. ICE control circuit 45 provides the internal control or timing signal for control circuit 45 (see Figs. 14 and 15). As indicated by Figs. 14 and 15, when supply voltage

V_{DD} is equal to or higher than V_{DT30}, ICE circuit 45 becomes operational at t1. At t2, V_{DD} is equal to or higher than V_{DT31}, and circuit 44 becomes operational, as indicated by the WL signal. When V_{DD} is equal to or lower than V_{DT31} (see Fig. 14, at t11 and Fig. 15, in between t9 and t10), the on-going sequence is allowed to finish (see Fig. 14, t11 and t12 and Fig. 15, t9 and t10), and a new operational sequence is prevented (see Col. 11, lines 5 - 16). When V_{DD} is equal to or lower than V_{DT30}, operation is immediately suspended (see Col. 11, lines 10 - 13). Consequently, Hirano's power-on/off circuit uses the same V_{DT31} to activate and deactivate ICE control circuit 45 and the same V_{DT30} to activate and deactivate control circuit 44.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify power-on/off reset circuit 14 of Hanaoka as taught by Hirano because Hirano's power-on/off reset circuit enables the memory circuit to properly terminate a sequence in operation when the voltage supply begins to drop below a predetermined voltage (see Hirano, Col. 2, lines 44 0 55).

7. Claims 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,521,590 (Hanaoka et al.) in view of U.S. Patent No. 5,973,598 (Beigel).

Regarding Claims 9 and 10, as explained above in Claims 5 - 8, it is understood that components 2 - 10 and 13 - 15 of data carrier 200 or RFID device, as shown in Figs. 4 and 5, form an integrated circuit element. Hanaoka's integrated circuit element comprises: modulator circuit 2 or communication means, control circuit 10 or logic processing means, and power-on reset circuit 14 for releasing control circuit 10 from an inactive state (see Col. 9, lines 62 - 65; Col. 10, lines 24 - 25 and 67; and Col. 11, lines 1 - 3). Hanaoka's data carrier 200 further comprises coil 1 for receiving power and signals from an external apparatus and for supplying power and signals to memory circuit 9 and control circuit 10 (see Col. 9, lines 50 - 54 and Col. 11, lines 7 -

19). When a voltage applied to power-on reset circuit 14 is lower than a threshold value, voltage detector circuit 13 causes switch 15 to cease supplying power to data carrier main circuit 100, causing data carrier 200 to become inactive (see Col. 10, lines 58 - 62). When data carrier 200 is inactive, its impedance state is decreased to a low state because the impedance level during inactivity is lower than the average impedance level during data transmission. However, when a reset state is release, signal transmission is performed by modulator circuit 2 changing the impedance between the induced voltage line V_{ac} and the reference potential line V_{dd} according to the data ($DATA_{out}$) read from memory circuit 9, thus resulting in changing an AC magnetic field emitted from coil 1 (see Col. 11, lines 14 - 19). As shown in Fig. 8, Hanaoka's modulator circuit 2 comprises a p-channel MOS transistor T1 or switching element, which is repeatedly turned on and off according to the data read from memory circuit 9 and causes the impedance between V_{ac} and V_{dd} to alternate between a high state and a low state (see Col. 11, lines 14 - 19 and Col. 12, lines 1 - 5). Hanaoka's modulator circuit 2, however, lacks a load resistor that has one terminal connected to coil 1 and the other terminal connected to the ground via transistor T1.

In an analogous art, Beigel's RFID tag, as shown in Figs. 7, 8A, and 8B, comprises a signal generator circuitry 78 that outputs an identification signal, which activate load circuit 90 in a predetermined sequence (see Col. 6, lines 9 - 15). Beigel imparts that load circuit 90 preferably comprises of a field effect transistor (FET) and a load resistor (see Col. 6, lines 13 - 14). As shown in Figs. 8A and 8B, load circuit 90 is connected signal generator circuitry 78, antenna 24, and ground 88. Here it is understood that one terminal of the load resistor is connected to antenna 24 and that the other terminal of the load resistor is connected to ground 88 via the FET.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Hanaoka's modulator circuit 2 as taught by Beigel because the use of a load resistor connected to a transistor provides signal amplification, thereby improving system reliability by amplifying data carrier 200's output signal, and is conventional and well known to those of ordinary skill in the art.

Regarding Claim 12, Hanaoka states that data carrier 200 includes non-contact integrated circuit (IC) cards (see Col. 1, lines 5 - 9).

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clara Yang whose telephone number is (703) 305-4086. The examiner can normally be reached on 8:30 AM - 7:00 PM, Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (703) 305-4704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CY
17 February 2004

BRIAN ZIMMERMAN
PRIMARY EXAMINER